NAME DATE STARTED TARGET END DATE

GCE AS LEVEL — COMPUTER SCIENCE UNIT 1 QUESTION PACK

2500U10-1 · 2015 spec Unit 1 Topic 2 · AS unit, first sat 2017, 100 marks, 2h paper

REVISE.wales

COMPUTER SCIENCE — UNIT 1 · Hardware — CPU, Memory & Storage

Topic 1.1 — Processor components, fetch-decode-execute, RAM, hard disk drives and peripheral devices

Von Neumann architecture, MAR/MDR/PC/CIR registers, the fetch-decode-execute cycle, parallel processing and caching, functional characteristics of HDDs vs optical drives, file fragmentation, and contemporary input devices.

2015 specification · current

Estimated time for entire question pack: ~1 h 30 min

Derived from the Unit 1 pace of ~1.2 min/mark, padded for written-prose answers (60 marks over 8 questions).

*You are advised to **not** attempt to complete all of this in one sitting.*

ABOUT THIS QUESTION PACK

This is a **comprehensive topic question pack**, not a single mock paper. It contains every question from the WJEC AS Unit 1 papers (Summer 2017 – Summer 2024, COVID gap) that maps onto Topic 1.1 of the 2015 specification.

Questions are ordered by source paper date.

INSTRUCTIONS

Use black ink or black ball-point pen. Show all working. A calculator is allowed where useful.

For Examiner's use only

Q	Source	Max	Mark
1	S17 Q2	10	
2	S18 Q7	5	
3	S19 Q3	6	
4	S19 Q4	10	

Q	Source	Max	Mark
5	S22 Q1	4	
6	S22 Q2	8	
7	S23 Q2	8	
8	S23 Q4	9	
Total		**60**	

Hardware — CPU, Memory & Storage — what the spec asks

WJEC GCE AS Computer Science (from 2015) · Unit 1: Fundamentals of Computer Science · Topic 1.1.

Von Neumann CPU components

- ALU performs arithmetic and logic operations.
- Control unit decodes instructions and coordinates other components via control bus.
- Registers (general purpose + special: PC, MAR, MDR, CIR, ACC).
- Internal buses link components; external buses link CPU to memory and I/O.

Special-purpose registers

- PC (Program Counter): address of next instruction to fetch.
- MAR (Memory Address Register): address being read from / written to RAM.
- MDR (Memory Data Register): the data going to or from RAM.
- CIR (Current Instruction Register): the instruction currently being decoded.

Fetch-decode-execute cycle

- Fetch: PC→MAR; RAM[MAR]→MDR; MDR→CIR; PC++.
- Decode: control unit interprets opcode and operand in CIR.
- Execute: ALU / control unit performs the operation; result to register or memory.
- Cycle repeats until HALT instruction.

Parallel processing & caching

- Multiple cores execute instructions in parallel → higher throughput.
- Pipelining overlaps fetch / decode / execute of consecutive instructions.
- Cache (L1, L2, L3): small fast SRAM holding recently used data and instructions.
- Cache hit avoids slow RAM access ⇒ large performance boost.

Hard Disk Drives (HDD)

- Magnetic platters spin at 5,400–15,000 rpm; read/write heads float on air cushion.
- Data stored on concentric tracks divided into sectors.
- Seek time + rotational latency + transfer time determine access time.
- Fragmentation slows access — defragmentation tools reorder file fragments.

Optical drives & peripherals

- Optical (CD/DVD/Blu-ray): laser reads pits on rotating disc; lower capacity than HDD but portable.
- Voice input: microphones + speech-recognition software; benefits include accessibility, hands-free.
- Touch input: capacitive or resistive screens; widely used on smartphones, kiosks.
- Trade-offs: speed, capacity, durability, cost, error rates.

Crib sheet »

Hardware — CPU, Memory & Storage in one page

Quick-reference notes — revisit before each question.

Register roles

PC: address of *next* instruction.
MAR: address being read / written.
MDR: data being moved.
CIR: current instruction.
ACC: accumulator (working value).

FDE cycle

1. PC → MAR
2. RAM[MAR] → MDR
3. MDR → CIR; PC++
4. Decode opcode in CIR
5. Execute (ALU / memory / I/O)
6. Repeat.

Cache hierarchy

L1 (small, fastest, per core) → L2 (larger, slightly slower) → L3 (largest, shared) → RAM → SSD/HDD.
Cache reduces average access time.

HDD access time

Seek + rotational latency + transfer.
Fragmentation increases seeks ⇒ slows access.
Defrag re-groups file blocks contiguously.

Word length

Word = bits CPU handles per operation.
32-bit ⇒ 4 GiB addressable RAM max.
64-bit ⇒ ~16 EB addressable; bigger integers, more registers.

Parallelism

Multi-core: independent instruction streams.
Pipelining: overlap FDE stages.
SIMD: same op on multiple data items.
Caching keeps the cores fed.

Examiner only

Answer **all** *questions.*

1. Complete the following truth table. [2]

A	B	A AND B	B XOR (A AND B)
0	0		
0	1		
1	0		
1	1		

2. Compare the functional characteristics of Hard Disc Drives (HDD) and Optical Drives and give a typical use and storage capacity for each. [10]

Examiner only

7. Certain central processing units (CPUs) use parallel processing and caching to improve performance.

Explain parallel processing and caching in a CPU. [5]

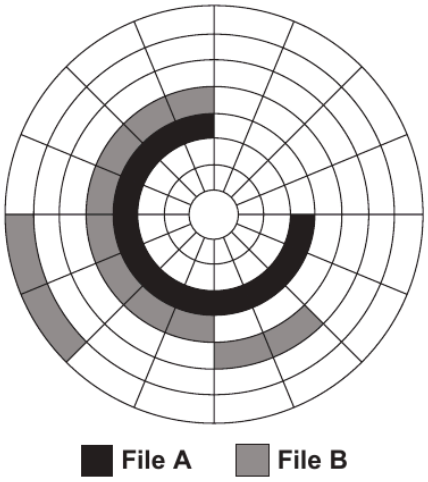
Examiner only

(b) Explain why this algorithm does not work as intended. [4]

3. Apart from buses, describe the function of **three** main components in a contemporary Von Neumann type CPU architecture. [6]

Examiner only

4. **Files A** and **B** are stored on an external hard disk drive (HDD).



(a) Describe the functional characteristics of a HDD. [5]

Examiner only

(b) (i) Explain why there would be a difference in disk access speeds when loading **File A** and **File B** into main memory. [3]

(ii) An alternative secondary storage medium which does not have the same issue as question *(b)*(i) is a Solid State Drive (SSD). Explain why this is the case. [2]

Examiner only

Answer **all** questions.

1. Describe the fetch-decode-execute cycle showing how data can be read from RAM into registers. Your answer should make reference to the MAR, MDR, PC and CIR. [4]

Examiner only

2. Describe the use of the following contemporary methods for input and their associated devices. Your answer should include their benefits and drawbacks.

(a) Voice input [4]

(b) Touch input [4]

Examiner only

2. A certain single-core processor will process the following calculation in seven steps:

$$Y = (4 \times 5) + (1 \times 6) + (5 \times 3) + (3 \times 2)$$

Step 1: $Y = 20 + (1 \times 6) + (5 \times 3) + (3 \times 2)$
Step 2: $Y = 20 + 6 + (5 \times 3) + (3 \times 2)$
Step 3: $Y = 20 + 6 + 15 + (3 \times 2)$
Step 4: $Y = 20 + 6 + 15 + 6$
Step 5: $Y = 26 + 15 + 6$
Step 6: $Y = 41 + 6$
Step 7: $Y = 47$

(a) (i) Describe, showing each step, how a quad-core processor would process the calculation. [3]

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(ii) State the name given to this method of processing data. [1]

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Examiner only

(b) Identify and state the purpose of **four** components in a CPU. [4]

Component 1

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Component 2

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Component 3

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Component 4

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Examiner only

4. (a) Explain, with reference to the functional characteristics of a Hard Disk Drive (HDD), how performance is affected by data fragmentation. [6]

(b) Describe how the effect of fragmentation can be reduced on a HDD. [3]

END OF QUESTION PACK

8 questions · 60 marks · ~1 h 30 min
Source: WJEC AS Computer Science Unit 1 (2500U10-1), Summer 2017–2024, COVID gap
Curated for WJEC Computer Science 2015 spec AS Unit 1 — Topic 2 (1.1)